ABSTRACT

A process is described to form a semiconductor device such as MOSFET or CMOS with shallow junctions in the source/drain extension regions. After forming the shallow trench isolations and the gate stack, sidewall dielectric spacers are removed. A pre-amorphizing implant (PAI) is performed with Ge^+ or Si^+ ions to form a thin PAI layer on the surface of the silicon regions adjacent to the gate stack. B^+ ion implantation is then performed to form source/drain extension (SDE) regions. The B^+ implant step is then followed by multiple-pulsed 248 nm KrF excimer laser anneal with pulse duration of 23 ns. This step is to reduce the sheet resistance of the junction through the activation of the boron dopant in the SDE junctions. Laser anneal is then followed by rapid thermal anneal (RTA) to repair the residual damage and also to induce out-diffusion of the boron to yield shallower junctions than the just-implanted junctions prior to RTA.